CLAIMS

What is claimed:

1. A semiconductor transistor comprising:

a layer having source and drain recesses formed therein with a channel between the source and drain recesses, and being made of a semiconductor material having a first lattice with a first structure and a first spacing;

a source and a drain formed in the source and drain recesses respectively, at least one of the source and the drain being made of a film material which:

(a) includes a dopant selected from one of a p-dopant and an n-dopant; and

(b) is formed epitaxially on the semiconductor material so as to have a second lattice having a second structure which is the same as the first structure, the second lattice having a second spacing which differs from the first spacing;

a gate dielectric layer on the channel; and

a conductive gate electrode on the gate dielectric layer.

2. The semiconductor transistor of claim 1 wherein:

(a) if the dopant is a p-dopant, the second spacing is larger than the first spacing; and

(b) if the dopant is an n-dopant, the second spacing is smaller than the

first spacing.

3. The semiconductor transistor of claim 1 wherein the difference between the first spacing and the second spacing creates a stress in the channel.

4. The semiconductor transistor of claim 1 wherein the second material includes the semiconductor material and an additive, the difference between the first spacing and the second spacing being due to the additive.

5. The semiconductor transistor of claim 4 wherein the semiconductor material is silicon and the additive is selected from one of germanium and carbon.

6. The semiconductor transistor of claim 5 wherein the additive is germanium.

7. The semiconductor transistor of claim 6 wherein the germanium comprises between 1 and 20 atomic percent of the silicon and the germanium of the film material.

8. The semiconductor transistor of claim 7 wherein the germanium

comprises approximately 15 atomic percent of the silicon and the germanium of the film material.

9. The semiconductor transistor of claim 4, further comprising:

tip regions formed between the source and the drain with the channel between the tip regions, the tip regions being formed by implanting of dopants and excluding the additive.

10. The semiconductor transistor of claim 9 wherein:

(a) if the dopant of the film material is a p-dopant, the dopants of the tip regions are p-dopants; and

(b) if the dopant of the film material is an n-dopant, the dopants of the tip regions are n-dopants.

11. The semiconductor transistor of claim 1 wherein the dopant comprises at least $0.5x10^{20}/cm^3$ of the film material.

12. The semiconductor transistor of claim 11 wherein the film material has a resistivity of less than 1.1mOhm-cm.

13. The semiconductor transistor of claim 1 wherein the source and drain

have a depth into the layer and are spaced by a width from one another, a ratio of the depth to the width being at least 0.12.

14. The semiconductor transistor of claim 13 wherein the ratio is at least 0.15.

15. The semiconductor transistor of claim 14 wherein the ratio is at least 0.2.

16. The semiconductor transistor of claim 15 wherein the ratio is at least 0.35.

17. The semiconductor transistor of claim 16 wherein the ratio is approximately $\frac{92}{215}$.

18. A semiconductor transistor comprising:

a layer having source and drain recesses formed therein with a channel between the source and drain recesses and being made of a semiconductor material having a first lattice with a first structure and a first spacing;

a source and a drain formed in the source and drain recesses respectively, at least one of the source and the drain being made of film material which:

(a) includes a dopant selected from one of a p-dopant and an n-dopant; and

(b) is formed epitaxially on the semiconductor material so as to have a second lattice having a second structure which is the same as the first structure; and

(i) if the dopant is a p-dopant, the second lattice has a second spacing which is larger than the first spacing, so that a compressive stress is created between the source and the drain in the channels; and

(ii) if the dopant is an n-dopant, the second lattice has a second spacing which is smaller than the first spacing, so that a tensile stress is created between the source and the drain in the channel;

a gate dielectric layer on the channel; and

a conductive gate electrode on the gate dielectric layer.

19. The semiconductor transistor of claim 18 wherein the film material includes the semiconductor material and an additive, wherein:

(a) if the dopant is a p-dopant, the second spacing is larger than the first spacing due to the additive; and

(b) if the dopant is an n-dopant, the second spacing is smaller than the first spacing due to the additive.

20. The semiconductor transistor of claim 19 wherein:

(a) if the dopant is a p-dopant, the additive is germanium; and

(b) if the dopant is an n-dopant, the additive is carbon.

21. A semiconductor transistor comprising:

a layer having source and drain recesses formed therein with a channel between the source and drain recesses, the layer being made of a semiconductor material;

a source and a drain formed in the source and drain recesses respectively, the source and the drain being made of a film material which includes a dopant selected from one of a p-dopant and an n-dopant, the source and the drain having a depth into the layer and being spaced by a width from one another, a ratio between the depth and the width being at least 0.12;

a gate dielectric layer on the channel; and

a conductive gate electrode on the gate dielectric layer.

22. The semiconductor transistor of claim 21 wherein the ratio is at least 0.35.

23. The semiconductor transistor of claim 21 wherein the depth is at least 80nm.

24. The semiconductor transistor of claim 21 wherein the width is less than 220nm.

25. A method of forming a transistor comprising:

forming a gate dielectric layer on a layer of semiconductor material;

forming a gate electrode on the gate dielectric layer;

implanting dopants into the layer of semiconductor material to form doped tip regions in the layer with a channel between the tip regions;

etching the layer to form source and drain recesses in the layer with the tip regions between the recesses; and

filling the source and drain recesses with a source and a drain respectively.

26. The method of claim 25 wherein at least one of the source and the drain is made of a film material which:

(a) includes a dopant selected from one of a p-dopant and an n-dopant; and

(b) is formed epitaxially on the semiconductor materials.

27. The method of claim 25 wherein the source and drain have a depth into the layer and are spaced by a width from one another, a ratio of the depth to the width being at least 0.12.